Attachment to Interview Summary

10/065,762 (JCLA8424)

Claims 的修正版本（二）

Claim 1 (currently amended) A buffer device, for transmitting a plurality of messages between a source controller and a destination controller, comprising:

a plurality of message rows, for storing the messages that the source controller intends to transmit to the destination controller, each of the message rows at least comprising a write complete flag and a distribution complete flag;

a write control unit, coupled between the source controller and the plurality of message rows, used to sequentially output a plurality of free message row addresses according to the plurality of distribution complete flags, wherein when the buffer device still has a free message row, the source controller reads an address of a target message row that is currently free among said plurality of message rows, and the distribution complete flag of the target message row is set by the write control unit; and when the source controller completes writing a message of the target message row, the write complete flag of the target message row is set by the write control unit, and a read request for informing the destination controller to read the message of the target message row is issued; and when the buffer device has no free message row, said write control unit outputs a non-free message row signal; and

a read control unit, coupled between the destination controller and the plurality of message rows, to issue the read request to inform the destination controller to read the message of the target message row when the write complete flag of the target message row is set by the write control unit, wherein once the destination controller completes reading the message of the target message row in response to the read request, the distribution complete flag set by the write control unit and the write complete flag set by the write control unit of the target message row are both cleared by the read control unit;

wherein the plurality of message rows are coupled between the write control unit and the read control unit.

Claim 2 (previously amended) The buffer device of claim 1, wherein the write control unit comprises:

a write pointer control unit, for storing a write address of the target message row, wherein after the source controller reads the write address of the target message row, said write pointer control unit sets the distribution complete flag of the target message row and progresses the write address, and when the source controller completes writing the message of the target message row, the write pointer control unit sets the write complete flag of the target message row;

a distribution complete flag multiplexer, coupled to the write pointer control unit and the distribution complete flags of the plurality of message rows, to output a not-distributed signal according to the distribution complete flag of the message row pointed to by the write address; and

a distribution address multiplexer, coupled to the distribution complete flag multiplexer and the write pointer control unit, to alternatively output one of the write address and the no free message row signal according to the not-distributed signal.

Claim 3 (previously amended) The buffer device of claim 1, wherein the read control unit comprises:

a read pointer control unit, to store a read address of the buffer device, wherein when the destination controller completes reading the message of the message row pointed to by the read address, said read pointer control unit clears the